REMARKS

Claims 1, 3, 4, 6-11, 13, 15, 17-21, 23, 24, 26, 28-31, 33, 34, 36, 38-40, 42, 43, 45, 47, 48, and 51 are pending in the present application and stand rejected. Claims 1, 6, 8, 9, 11, 21, 26, 28-31, 40, 45, 47, and 48 are amended and claim 51 is added. No new matter has been added. The Examiner's reconsideration is respectfully requested in view of the above amendments and the following remarks.

Claim Rejections – 35 U.S.C. 103(a)

1. Claims 1, 3-4, 6-7, 9, 11, 15, 18-19, 21, 25-26, 29,31, 33-36, 39-40, 42-43, and 45 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Circello [US Pat # 5,872,940] in view of Ryan [US Pat Pub # 2006/0277424] and in further view of Funk [US Pat # 6,026,119], as set forth in pages 2-9 of the Office Action.

Claim Amendments

Claims 1, 11, 21, 31, 40 have been amended to clarify a claimed bus master controller. The amendments are believed to at least be supported by FIG. 4 and paragraphs 37 and 38 of applicant's U.S. Patent Publication 2005/0066074.

Claim 1

It is respectfully submitted that Circello, Ryan, and Funk, alone or in combination, do not disclose or suggest a bus master controller that includes *a packet generator for receiving control signals from a protocol converter and protocol signal controller and a translated address from an address translator and packetizing the control signals and the translated address in a command packet*, and *a multiplexer for receiving the command packet from the packet generator*

and a data packet from a data pack unit and outputting one of the command packet or the data packet to the common bus, as recited in amended claim 1.

Circello teaches (in FIG. 5) a bus controller 103 that includes a pair of multiplexers 510 and 502, where multiplexer 502 receives a control signal (R/W) from a core 102 and multiplexer 510 receives an address signal.

However, no element of the bus controller 103 of Circello receives both a translated address and control signals and packetizes the control signals and the translated address in a command packet.

Even assuming *arguendo* that the output signal of multiplexer 510 input to the SELECT input of multiplexer 502 is interpreted as a translated address, the multiplexer 502 of Circello does not packetize the R/W signal and the output signal in a command packet. For example, the multiplexer 502 only outputs the R/W or an inverted form of R/W based on the output signal.

Further, neither of the multiplexers 502 or 510 of Circello receives both a command packet from a packet generator and a data packet from a data pack unit and output one of the command packet or the data packet to a common bus.

Circello (in FIG. 5 and col. 4, lines 5-21) teaches the multiplexer 502 only receiving individual bits 604, 608, 612 respectively from registers 603, 607, and 611, and not a command packet from a packet generator and a data packet form a data pack unit. The registers 603, 607, and 611 are not considered packet generators or pack units because they only output individual bits 604, 608, 612, and not packets. Further, the multiplexer 502 does not output one of a command packet or a data packet. For example, the multiplexer 502 merely outputs one of bits

604, 608, 612, and there is no teaching in Circello of the bits being derived from control signals and a translated address.

Circello (in FIG. 5) teaches the multiplexer 510 only receiving a R/W and an inverted R/W control signal from a Core 102, and not a command packet from a packet generator and data packet from a data packet unit. Further, Circello does not disclose the Core 102 packing data into packets and packeting the R/W control signals and a translated address into a command packet for output to multiplexer 502.

Thus, Circello fails to disclose or suggest, a bus master controller that includes *a packet generator for receiving control signals from a protocol converter and protocol signal controller and a translated address from an address translator and packetizing the control signals and the translated address in a command packet,* and *a multiplexer for receiving the command packet from the packet generator and a data packet from a data pack unit and outputting one of the command packet or the data packet to the common bus*, as recited in amended claim 1. The deficiencies of Circello in this regard are not cured by Ryan or Funk. For example, Ryan and Funk make no mention of a bus master controller, much less a bus master controller as described in claim 1.

Circello also fails to disclose *a protocol converter and protocol signal controller for receiving control signals from a central processing unit through a bus interface and managing control signal flow according to a present protocol, an address translator for receiving the address from the central processing unit through the bus interface and translating the address depending on an application module to be accessed, and a receive buffer for receiving data from the central processing unit through the bus interface*, as essentially recited in amended claim 1.

For example, bus master controller 103 of in FIG. 5 of Circello merely includes a pair of multiplexers 502, 510 and a plurality of registers 603, 607, 611. Further, there is no teaching in Circello of the multiplexers or registers being used as protocol converters, address translators, or buffers. Further, the deficiencies of Circello in these regard are not cured by Ryan and Funk.

For at least the foregoing reasons, claim 1 is believed to be patentable over the combination of Circello, Ryan, and Funk.

Claim 11

It is further respectfully that Circello, Ryan, and Funk do not disclose or suggest a bus master controller that includes *a packet generator for receiving control signals and an address, and packetizing the control signals and the address in a command packet, a data pack unit for packing data into a data packet, and a multiplexer for receiving the command packet from the packet generator and the data packet from the data pack unit and outputting one of the command packet or the data packet to the common bus*, as essentially recited in amended claim 11.

As shown in FIG. 5 of Circello, the bus master controller 103 of Circello does not include a packet generator or data packing unit. Further, no element in the bus master controller 103 forms a command packet out of control signals and an address. Even assuming *arguendo* that bits 604, 608, 612 are interpreted as control signals, multiplexer 510 does not combine them with the address to form a command packet (e.g, it only uses the address to select one of the bits for output). Even assuming *arguendo* that the output of multiplexer 510 to multiplexer 502 is interpreted as an address, multiplexer 502 does not combine the R/W signal and the output into a command packet (e.g., it only uses the output to select either the R/W signal or the inverted R/W signal for output).

Thus, Circello fails to disclose a bus master controller including *a packet generator for receiving control signals and an address, and packetizing the control signals and the address in a command packet, a data pack unit for packing data into a data packet, and a multiplexer for receiving the command packet from the packet generator and the data packet from the data pack unit and outputting one of the command packet or the data packet to the common bus*, as essentially recited in amended claim 11. The deficiencies of Circello in this regard are not cured by Ryan or Funk. For example, Ryan and Funk make no mention of a bus master controller, much less a bus master controller as described in claim 11.

Claims 21, 31, and 40 are believed to be patentable over said combination for at least similar reasons to claim 1. For example, a bus controller of claims 21, 31, and 40 has been amended in a similar manner to claim 1.

Dependent claims 3-4, 6-7, 11, 15, 18-19, 25-26, 29, 33-36, 39, 42-43, and 45 are believed to be patentable over said combination at least by virtue of their dependence from their respective base claims.

2. Claims 8, 17, 28, 38, and 47 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Circello, Ryan, Funk, and in further view of Watanabe [US Pat # 6,378,102], as set forth in pages 9-10 of the Office Action.

3. Claims 10 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Circello, Ryan, Funk, and in further view of Fueki [US Pat Pub # 2002/0166058], as set forth in pages 10-11 of the Office Action.

4. Claim 13 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Circello, Ryan, Funk , and in further view of Wilska [US Pat Pub # 2002/0082043], as set forth in page 11-12 of the Office Action.

The above 103 rejections (i.e., 2-4) are premised, in part, on the Examiner's reliance on Circello, Ryan and Funk, as disclosing all elements of claim 1, 11, 21, 31, and 40, where claims 8 and 10 depend from claim 1, claims 13, 17, and 20 depend from claim 11, claim 28 depends from claim 21, claim 38 depends from claim 31, and claim 47 depends from claim 40.

However, Circello, Ryan and Funk do not disclose all of the limitations of claims 1, 11, 21, 31, and 40 for at least the reasons discussed above. Further, the deficiencies of Circello, Ryan and Funk in disclosing claims 1, 11, 21, 31, and 40 are not cured by Watanabe, Fueki, or Wilska. For example, at the very least, Watanabe, Fueki, and Wilska fail to disclose or suggest a bus master controller that includes a packet generator for receiving control signals and an address and packetizing the control signals and the address in a command packet, and a multiplexer for receiving the command packet from the packet generator and a data packet from a data pack unit and outputting one of the command packet or the data packet to a common bus.

Accordingly, the above respective combinations of Circello, Ryan, Funk, Watanabe, Fueki, and Wilska cannot render obvious any of the above claims rejected under 35 U.S.C. 103(a).

Newly Added Claim

Newly added claim 51 is believed to be patentable over any of the cited art by virtue of its dependence from claim 11 and for the reasons above discussed for claim 1.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,
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